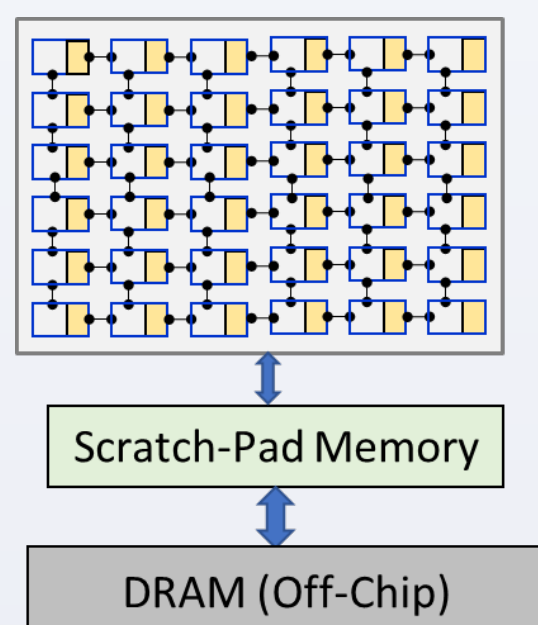
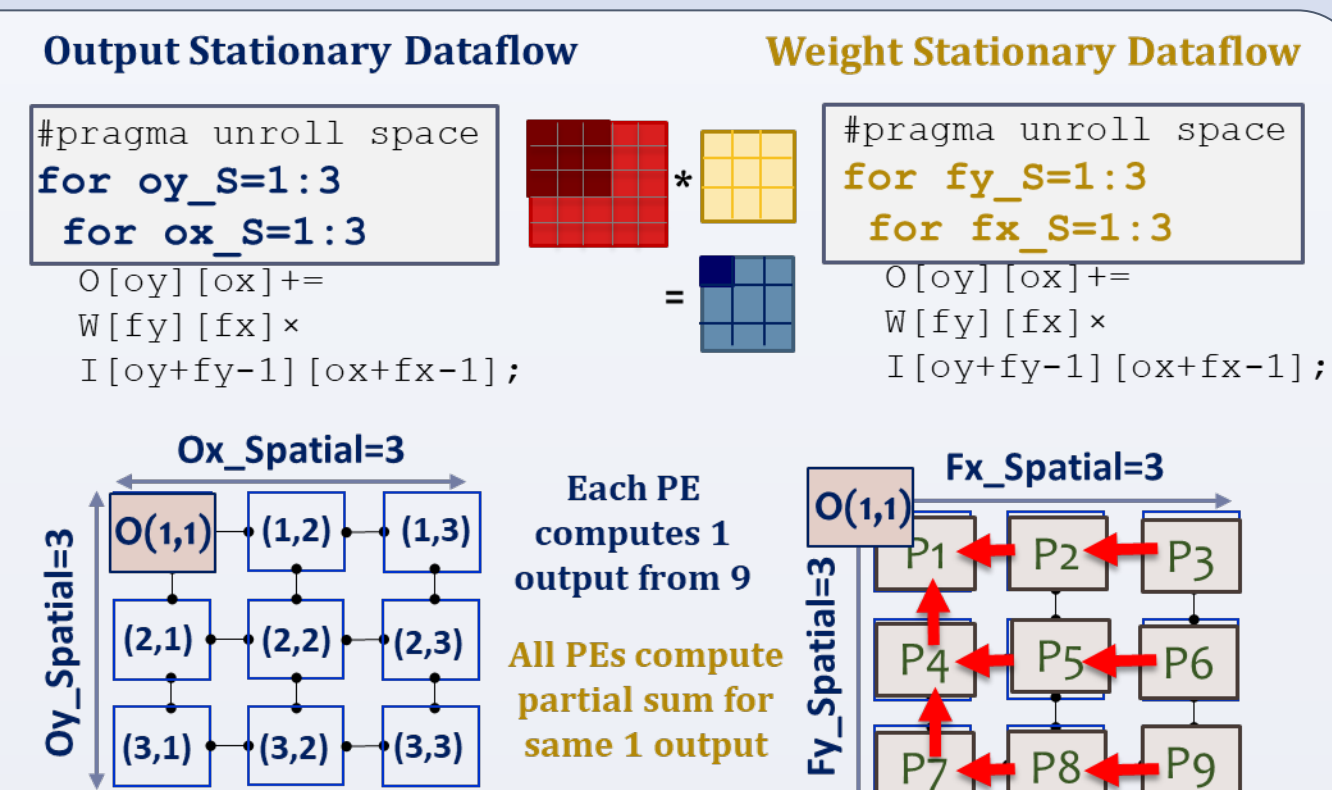


Programmable Dataflow Accelerators

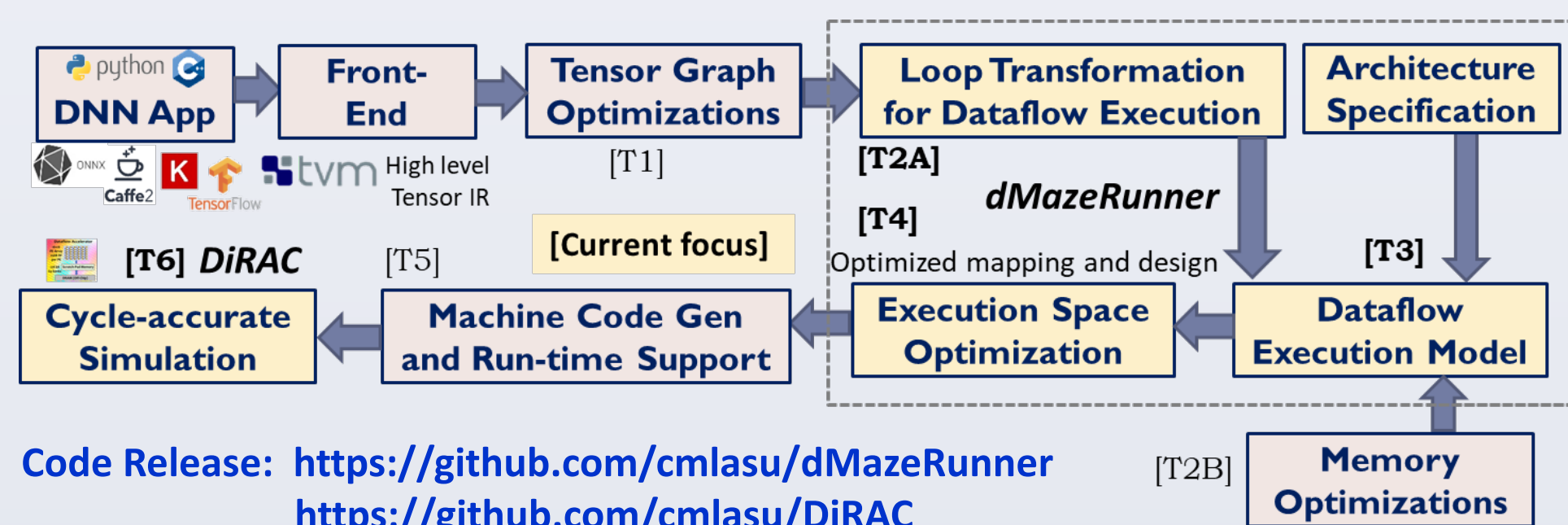
- **Massive array of Processing Elements (PEs);** each PE has ALU-like functional unit to perform operation every cycle (**simple, programmable**).
- PE's Private + shared memory sustain data reuse.
- **Efficiently accelerate ML and media kernels.**
- Architecture Variations
 - Systolic arrays: TPU (Google), TensorCore (nVIDIA)
 - Spatially programmable architecture: Eyeriss (MIT), SCNN (nVIDIA), AI core (IBM), CSA (Intel)
 - Coarse-grained reconfig array: HyCUBE(NUS), DPU(Wave)



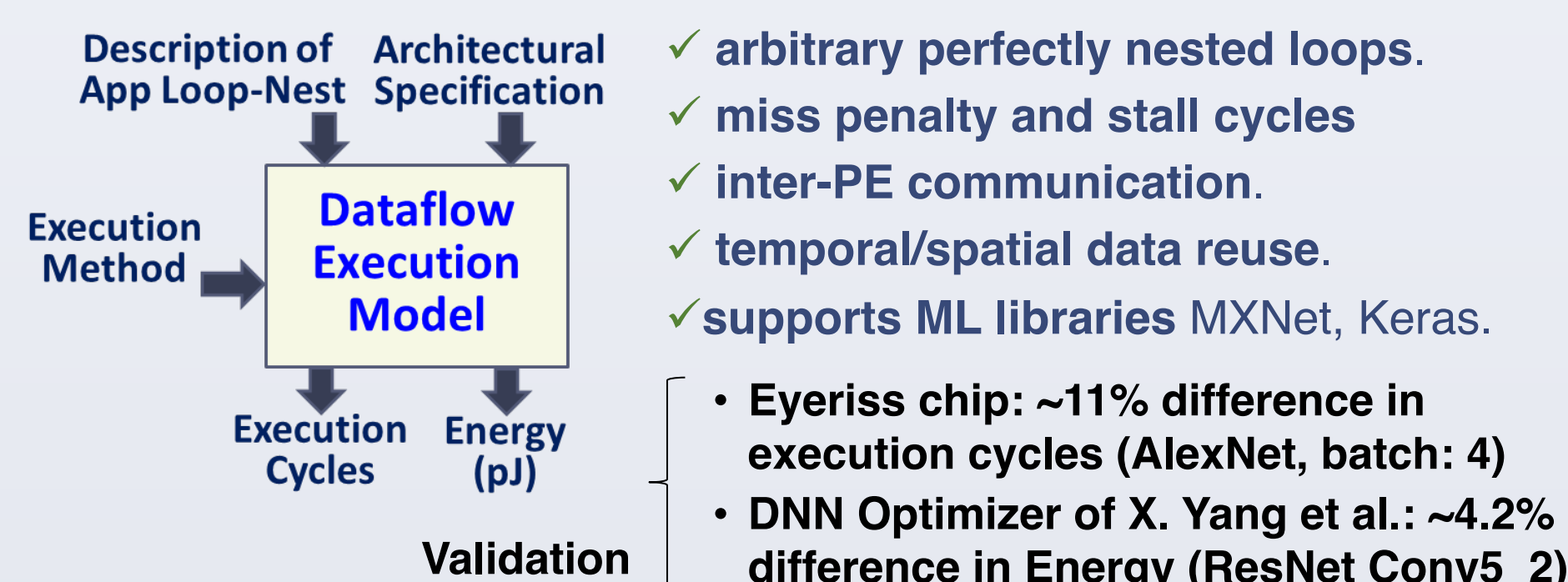
SpatioTemporal Execution of Loops



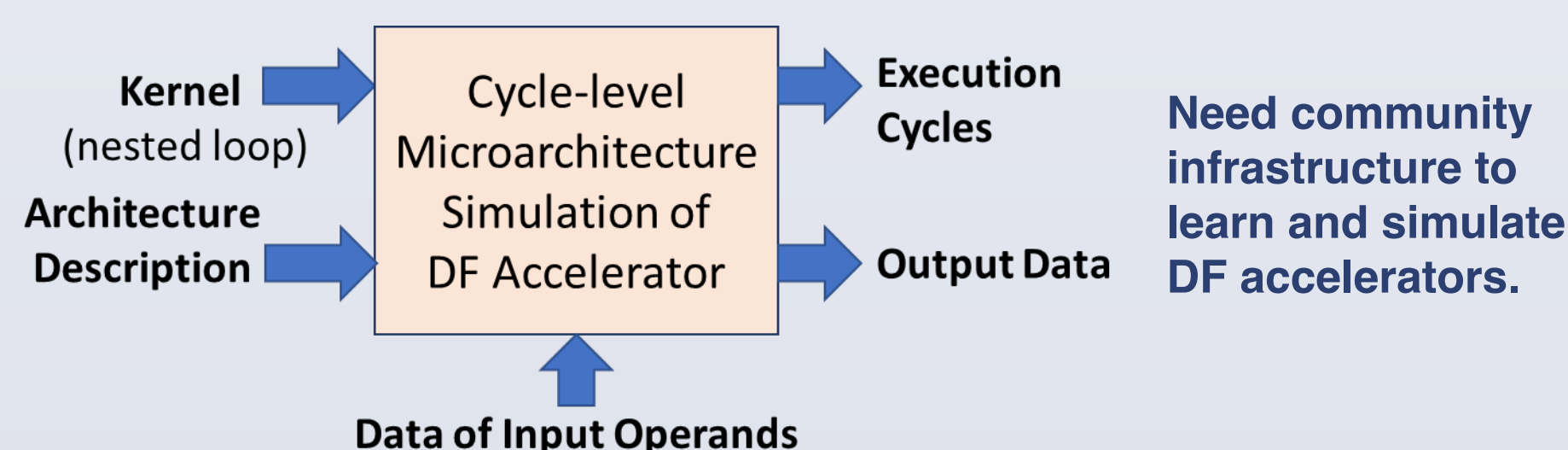
Current Focus in System Stack



Analytical Model of Dataflow Execution



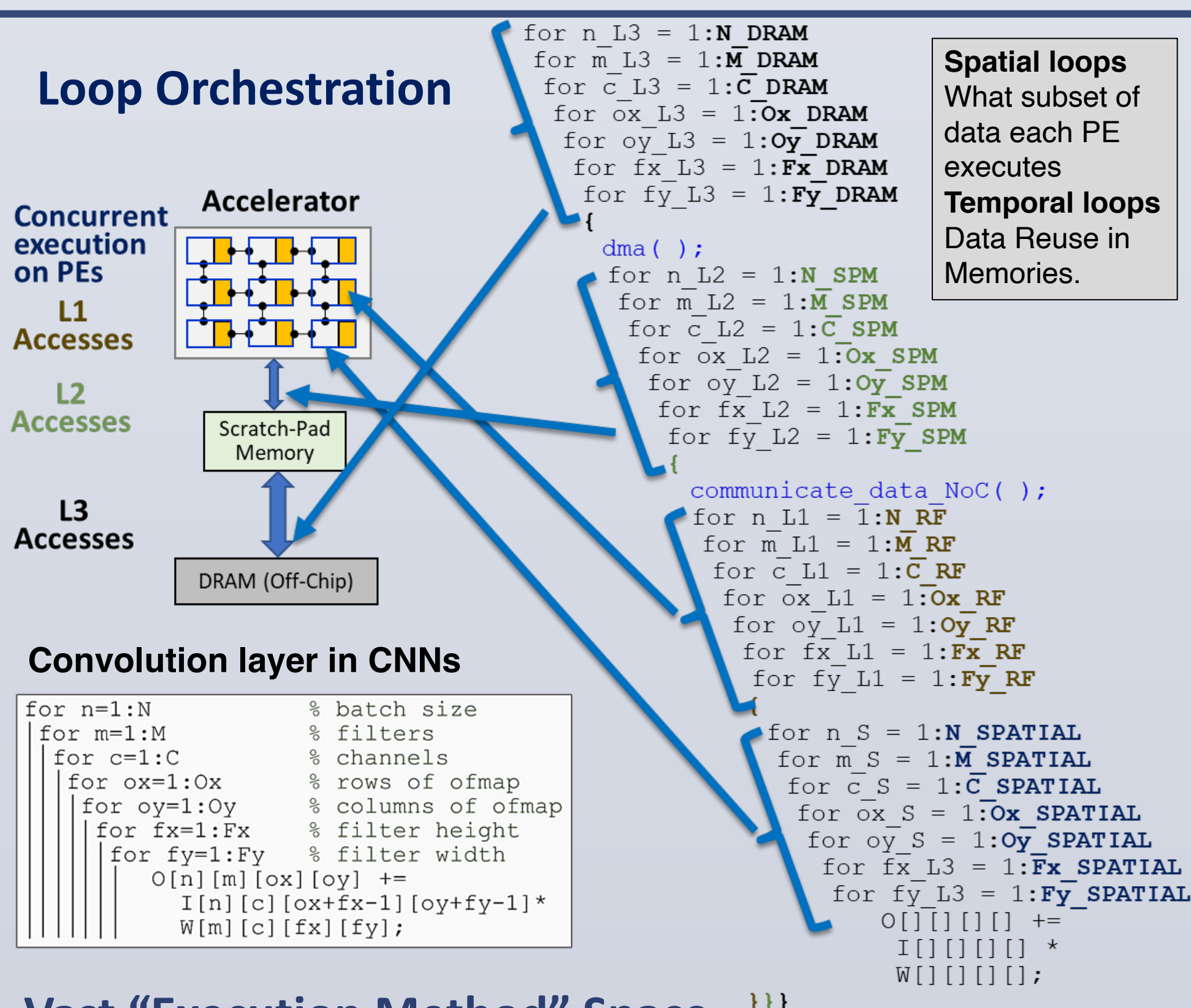
DiRAC: Cycle-level march Simulation



- **DiRAC:** `--path test_conv_output_stationary --cmp-golden 1`

- Architecture variations: PE grid layout, PE pipeline, size/buffering/partitioning of Register Files and Scratchpad memory, interconnect, DMA configuration
- Simulate nested loops with no conditional statements and with MAC operations.

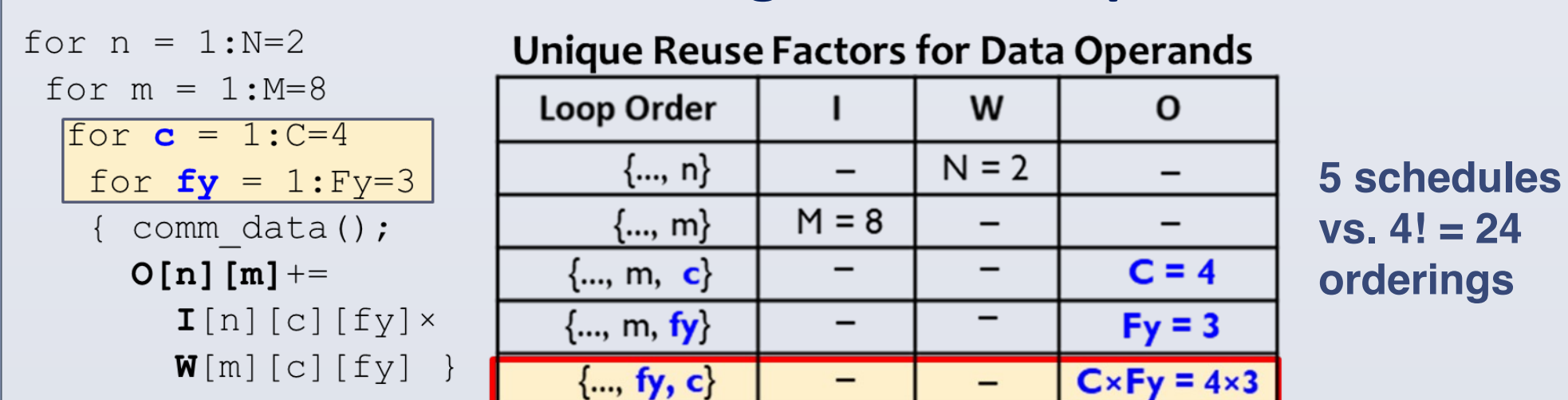
Loop Orchestration



Vast "Execution Method" Space

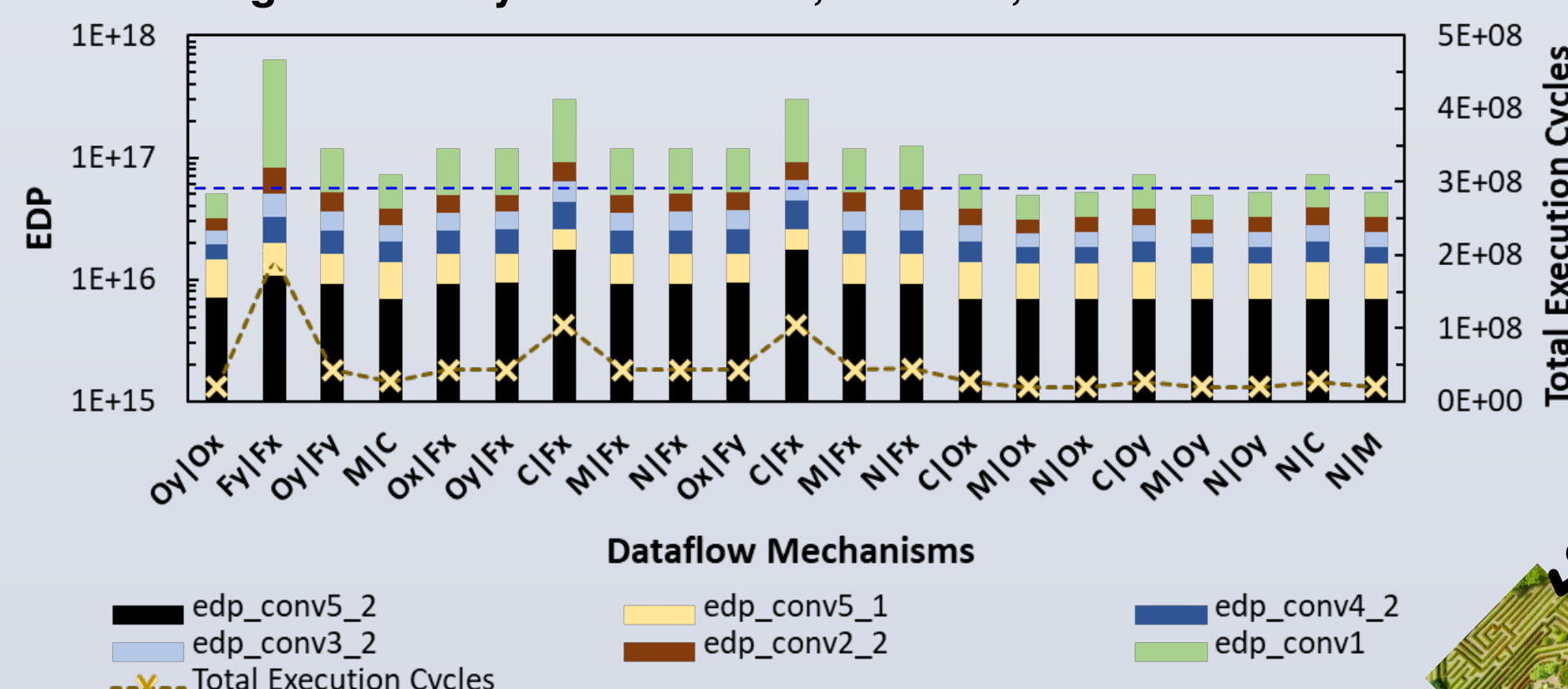
Problem of exploring "execution methods" becomes problem of exploring all the possibilities of tiling and ordering in 28-dimensional loop.

Drastic Pruning of Search Space



Results: Optimized Mappings Across DFs and Layers

Executing ResNet layers on 256-PE, 512B RF, 128kB SPM accelerator



Adaptable Mappings = Better Results

- Optimize various factors
- ✓ Very high resource utilization
 - ✓ Reuse of multiple operands
 - ✓ Minimize DRAM accesses.
 - ✓ Efficiently interleave compute with communication latency

dMazeRunner Features

- Non-expert programmers can explore space in seconds.
- Domain experts can perform directed search.
- Explore efficient designs for models/layers through DSE

```
python run_optimizer.py
--frontend mxnet --model
resnet18_v1 -auto-optimize
```

Acknowledgements

This work was partially supported by funding from NSF grant CCF 1723476 – NSF/Intel joint research center for Computer Assisted Programming for Heterogeneous Architectures (CAPA) and from the grants NRF-2015M3C4A7065522 and 2014-3-00035 funded by MSIT.